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L2	7348	L1 and translat$4	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/11/14 12:27
L3	4988	L2 and @ad<"20011222"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/11/14 12:28
L4	4534	L3 and computer	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/11/14 12:28
L5	3156	"L5" and optimiz$7	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/11/14 12:30
L9	1963	L5 and @ad>"20010101"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/11/14 12:33
L10	1198	L5 and @ad<"20010101"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/11/14 13:20
L12	7	L5 and (emulat$5.ti. or emulat$5. ab.)	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/11/14 12:35
S1	320	703/26.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/11/13 12:20
S2	295	S1 and @ad<"20020101"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/11/14 12:23

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» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

1. **Neural dynamic optimization for control systems.III. Applications**
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AbstractPlus | Full Text: PDF(32 KB) IEEE CNF

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IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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Volume 33, Issue 3, March 2000 Page(s):47 - 52
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10. **Dynamic binary translation and optimization**
Ebcioglu, K.; Altman, E.; Gschwind, M.; Sathaye, S.;
Computers, IEEE Transactions on
Volume 50, Issue 6, June 2001 Page(s):529 - 548
Digital Object Identifier 10.1109/12.931892

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1 Optimizations and oracle parallelism with dynamic translation

Kemal Ebcioğlu, Erik R. Altman, Michael Gschwind, Sumedh Sathaye

November 1999 **Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available: pdf(1.28 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We describe several optimizations which can be employed in a dynamic binary translation (DBT) system, where low compilation/translation overhead is essential. These optimizations achieve a high degree of ILP, sometimes even surpassing a static compiler employing more sophisticated, and more time-consuming algorithms [9]. We present results in which we employ these optimizations in a dynamic binary translation system capable of computing oracle parallelism.

2 Optimizing direct threaded code by selective inlining

Ian Piumarta, Fabio Riccardi

May 1998 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1998 conference on Programming language design and implementation PLDI '98**, Volume 33 Issue 5

Publisher: ACM Press

Full text available: pdf(1.28 MB) Additional Information: full citation, abstract, references, citings, index terms

Achieving good performance in bytecoded language interpreters is difficult without sacrificing both simplicity and portability. This is due to the complexity of dynamic translation ("just-in-time compilation") of bytecodes into native code, which is the mechanism employed universally by high-performance interpreters.We demonstrate that a few simple techniques make it possible to create highly-portable dynamic translators that can attain as much as 70% the performance of optimized C for certain n ...

Keywords: bytecode interpretation, dynamic translation, inlining, just-in-time compilation, threaded code

3 Machine-adaptable dynamic binary translation

David Ung, Cristina Cifuentes

January 2000 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN workshop on Dynamic and adaptive compilation and optimization DYNAMO '00**, Volume 35 Issue 7

Publisher: ACM Press

Full text available: pdf(1.23 MB) Additional Information: full citation, abstract, references, citings, index terms

Dynamic binary translation is the process of translating and optimizing executable code for one machine to another at runtime, while the program is "executing" on the target machine.

Dynamic translation techniques have normally been limited to two particular machines; a competitor's machine and the hardware manufacturer's machine. This research provides for a more general framework for dynamic translations, by providing a framework based on specifications of machines that ...

Keywords: binary translation, dynamic compilation, dynamic execution, emulation, interpretation

4 Dynamo: a transparent dynamic optimization system

Vasanth Bala, Evelyn Duesterwald, Sanjeev Banerjia
May 2000 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2000 conference on Programming language design and implementation PLDI '00**, Volume 35 Issue 5
Publisher: ACM Press

Full text available: pdf(156.03 KB) Additional Information: full citation, abstract, references, citings, index terms

We describe the design and implementation of Dynamo, a software dynamic optimization system that is capable of transparently improving the performance of a native instruction stream as it executes on the processor. The input native instruction stream to Dynamo can be dynamically generated (by a JIT for example), or it can come from the execution of a statically compiled native binary. This paper evaluates the Dynamo system in the latter, more challenging situation, in order to emphasize the ...

5 Binary translation and architecture convergence issues for IBM system/390

Michael Gschwind, Kemal Ebcioğlu, Erik Altman, Sumedh Sathaye
May 2000 **Proceedings of the 14th international conference on Supercomputing**
Publisher: ACM Press

Full text available: pdf(1.44 MB) Additional Information: full citation, abstract, references, index terms

We describe the design issues in an implementation of the ESA/390 architecture based on binary translation to a very long instruction word (VLIW) processor. During binary translation, complex ESA/390 instructions are decomposed into instruction "primitives" which are then scheduled onto a wide-issue machine. The aim is to achieve high instruction level parallelism due to the increased scheduling and optimization opportunities which can be exploited by binary translation software ...

6 Increasing the size of atomic instruction blocks using control flow assertions

Sanjay J. Patel, Tony Tung, Satarupa Bose, Matthew M. Crum
December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**
Publisher: ACM Press

Full text available: pdf(140.81 KB) ps(646.25 KB) Publisher Site Additional Information: full citation, references, citings, index terms

7 Back to the future: the story of Squeak, a practical Smalltalk written in itself

Dan Ingalls, Ted Kaehler, John Maloney, Scott Wallace, Alan Kay
October 1997 **ACM SIGPLAN Notices , Proceedings of the 12th ACM SIGPLAN conference on Object-oriented programming, systems, languages, and applications OOPSLA '97**, Volume 32 Issue 10

Publisher: ACM Press

Full text available: pdf(1.28 MB) Additional Information: full citation, abstract, references, citings, index terms

Squeak is an open, highly-portable Smalltalk implementation whose virtual machine is written entirely in Smalltalk, making it easy to. debug, analyze, and change. To achieve practical performance, a translator produces an equivalent C program whose performance is comparable to commercial Smalltalks.Other noteworthy aspects of Squeak include: a compact object format that typically requires only a single word of overhead per object; a simple yet efficient incremental garbage collector for 32-bit d ...

8 Optimization and precise exceptions in dynamic compilation

Michael Gschwind, Erik Altman

March 2001 **ACM SIGARCH Computer Architecture News**, Volume 29 Issue 1

Publisher: ACM Press

Full text available: pdf(508.52 KB) Additional Information: full citation, abstract, index terms

Maintaining precise exceptions is an important aspect of achieving full compatibility with a legacy architecture. While asynchronous exceptions can be deferred to an appropriate boundary in the code, synchronous exceptions must be taken when they occur. This introduces uncertainty into liveness analysis since processor state that is otherwise dead may be exposed when an exception handler is invoked. Previous systems either had to sacrifice full compatibility to achieve more freedom to perform op ...

9 Understanding the backward slices of performance degrading instructions

Craig B. Zilles, Gurindar S. Sohi

May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture ISCA '00**, Volume 28 Issue 2

Publisher: ACM Press

Full text available: pdf(128.47 KB) Additional Information: full citation, abstract, references, citings, index terms

For many applications, branch mispredictions and cache misses limit a processor's performance to a level well below its peak instruction throughput. A small fraction of static instructions, whose behavior cannot be anticipated using current branch predictors and caches, contribute a large fraction of such performance degrading events. This paper analyzes the dynamic instruction stream leading up to these performance degrading instructions to identify the operations necessary to exec ...

10 An efficient implementation of SELF a dynamically-typed object-oriented language based on prototypes

C. Chambers, D. Ungar, E. Lee

September 1989 **ACM SIGPLAN Notices , Conference proceedings on Object-oriented programming systems, languages and applications OOPSLA '89**, Volume 24 Issue 10

Publisher: ACM Press

Full text available: pdf(2.41 MB) Additional Information: full citation, abstract, references, citings, index terms

We have developed and implemented techniques that double the performance of dynamically-typed object-oriented languages. Our SELF implementation runs twice as fast as the fastest Smalltalk implementation, despite SELF's lack of classes and explicit variables. To compensate for the absence of classes, our system uses implementation-level maps to transparently group objects cloned from the same prototype, providing data type information and eliminating the apparent ...

11 Options for dynamic address translation in COMAs

Xiaogang Qiu, Michel Dubois

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture ISCA '98**, Volume 26 Issue 3

Publisher: IEEE Computer Society, ACM Press

Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, citings, index terms

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In modern processors, the dynamic translation of virtual addresses to support virtual memory is done before or in parallel with the first-level cache access. As processor technology improves at a rapid pace and the working sets of new applications grow insatiably the latency and bandwidth demands on the TLB (Translation Lookaside Buffer) are getting more and more difficult to meet. The situation is worse in multiprocessor systems, which run larger applications and are plagued by the TLB consiste ...

12 The Jalapeño dynamic optimizing compiler for Java

Michael G. Burke, Jong-Deok Choi, Stephen Fink, David Grove, Michael Hind, Vivek Sarkar, Mauricio J. Serrano, V. C. Sreedhar, Harini Srinivasan, John Whaley

June 1999 **Proceedings of the ACM 1999 conference on Java Grande**

Publisher: ACM Press

Full text available: pdf(1.34 MB) Additional Information: full citation, references, citings, index terms

13 Making pure object-oriented languages practical

Craig Chambers, David Ungar

November 1991 **ACM SIGPLAN Notices , Conference proceedings on Object-oriented programming systems, languages, and applications OOPSLA '91**, Volume 26 Issue 11

Publisher: ACM Press

Full text available: pdf(1.86 MB) Additional Information: full citation, references, citings, index terms

14 Embra: fast and flexible machine simulation

Emmett Witchel, Mendel Rosenblum

May 1996 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1996 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '96**, Volume 24 Issue 1

Publisher: ACM Press

Full text available: pdf(1.83 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes Embra, a simulator for the processors, caches, and memory systems of uniprocessors and cache-coherent multiprocessors. When running as part of the SimOS simulation environment, Embra models the processors of a MIPS R3000/R4000 machine faithfully enough to run a commercial operating system and arbitrary user applications. To achieve high simulation speed, Embra uses dynamic binary translation to generate code sequences which simulate the workload. It is the first machine simu ...

15 Efficient implementation of the smalltalk-80 system

L. Peter Deutsch, Allan M. Schiffman

January 1984 **Proceedings of the 11th ACM SIGACT-SIGPLAN symposium on Principles of programming languages**

Publisher: ACM Press

Full text available: pdf(595.22 KB) Additional Information: full citation, abstract, references, citings, index terms

The Smalltalk-80* programming language includes dynamic storage allocation, full upward funargs, and universally polymorphic procedures; the Smalltalk-80 programming system features interactive execution with incremental compilation, and implementation portability. These features of modern programming systems are among the most difficult to implement efficiently, even individually. A new implementation of the Smalltalk-80 system, hosted on a small microprocessor-based computer, achieves hig ...

16 Customization: optimizing compiler technology for SELF, a dynamically-typed object-oriented programming language

C. Chambers, D. Ungar

June 1989 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1989 Conference on Programming language design and implementation PLDI '89**, Volume 24 Issue 7

Publisher: ACM Press

Full text available: pdf(1.87 MB) Additional Information: full citation, abstract, references, citings, index terms

Dynamically-typed object-oriented languages please programmers, but their lack of static type information penalizes performance. Our new implementation techniques extract static type information from declaration-free programs. Our system compiles several copies of a given procedure, each customized for one receiver type, so that the type of the receiver is bound at compile time. The compiler predicts types that are statically unknown but likely, and inserts ...

17 Clarity MCode: a retargetable intermediate representation for compilation

Brian T. Lewis, L. Peter Deutsch, Theodore C. Goldstein

March 1995 **ACM SIGPLAN Notices , Papers from the 1995 ACM SIGPLAN workshop on Intermediate representations**, Volume 30 Issue 3

Publisher: ACM Press

Full text available: pdf(948.64 KB) Additional Information: full citation, citings, index terms

18 Migrating a CISC computer family onto RISC via object code translation

Kristy Andrews, Duane Sand

September 1992 **ACM SIGPLAN Notices , Proceedings of the fifth international conference on Architectural support for programming languages and operating systems ASPLOS-V**, Volume 27 Issue 9

Publisher: ACM Press

Full text available: pdf(1.13 MB) Additional Information: full citation, references, citings, index terms

19 BrouHaHa- A portable Smalltalk interpreter

Eliot Miranda

December 1987 **ACM SIGPLAN Notices , Conference proceedings on Object-oriented programming systems, languages and applications OOPSLA '87**, Volume 22 Issue 12

Publisher: ACM Press

Full text available: pdf(1.10 MB) Additional Information: full citation, abstract, references, citings, index terms

BrouHaHa is a portable implementation of the Smalltalk-80 virtual machine interpreter. It is a more efficient redesign of the standard Smalltalk specification, and is tailored to suit conventional 32 bit microprocessors. This paper presents the major design changes and optimization techniques used in the BrouHaHa interpreter. The interpreter runs at 30% of the speed of the Dorado on a Sun 3/160 workstation. The implementation is portable because it is written in C.

20 PACT 2001 workshops: Workshop on binary translation - 2001

Erik R. Altman, David R. Kaeli

December 2001 **ACM SIGARCH Computer Architecture News**, Volume 29 Issue 5

Publisher: ACM Press

Full text available: pdf(124.74 KB) Additional Information: full citation, index terms

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